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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,265	03/12/2004	Tyler Lowrey	2024.46	7228

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EXAMINER

CAO, PHAT X

ART UNIT	PAPER NUMBER
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2814

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/799,265

Applicant(s)

LOWREY ET AL.

Examiner

Phat X. Cao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,7-9,16-23,25,26,29-33,35,36,39-53 and 58-87 is/are pending in the application.
- 4a) Of the above claim(s) 76-87 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,7-9,16-23,25,26,29-33,35,36,39-53,58-75 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The cancellation of claims 2-6, 10-15, 24, 27-28, 34, 37-38, and 54-57 in Paper filed on 1/19/07 is acknowledged.
2. Newly submitted claims 76-87 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

The invention originally claimed does not require the steps of forming a cell area less than $8F^2$ and utilizing three or less masking steps as claimed in new claims 76-79, the steps of forming a cell area less than $6F^2$ and utilizing three or less masking steps as claimed in new claims 80-83, or the steps of forming a non-charge-storage comprising utilizing three or less steps as claimed in new claims 84-87.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 76-87 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2814

4. Claims 1, 7-9, 16-23, 25-26, 29-33, 35-36, 39-53, 58-60, 63-65, 68-69, and 72-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita (Us. 5,529,956) in view of Harshfield (US. 6,031,287).

Regarding claims 1, 7-8, 18, 20, 23, 30, 33, 41, 47 and 53, Morishita (Figs. 1A 1G) discloses a method of making an electrically contact element, comprising: providing a first dielectric layer 4, the first dielectric layer 4 having an opening, the opening having a sidewall surface and a bottom surface; forming a conductive layer 10 on the sidewall surface and on a portion of the bottom surface of the opening, the portion being less than the entire bottom surface (Fig. 1D); forming a second dielectric layer 11 over the conductive layer 10 and at least a portion of the bottom surface (also See Fig. 1D); and forming upper level wiring conductor 7 in electrical communication with the conductive layer 10.

Morishita does not disclose that the upper level-wiring conductor 7 is a phase-change programmable resistance material made of chalcogenide.

However, Harshfield (Fig. 24) teaches the forming of a phase-change programmable resistance material 130 of chalcogenide (column 7, lines 5-12 and column 14, lines 1-5) as an upper level-wiring conductor in electrical communication with a lower level-wiring conductor 106 through a conductive layer 124 (column 13, lines 48-51 and lines 66-67). Accordingly, it would have been obvious to modify the method of Morishita by forming the upper level wiring conductor 7 with a phase-change programmable resistance material because such a forming of the phase-change programmable resistance material for the upper level wiring conductor would provide a

Art Unit: 2814

memory cell for a programmable memory device, as taught by Harshfield (column 14, lines 1-5).

Regarding claims 9, 29 and 39, Morishita does not disclose that the first dielectric layer 4 and the second dielectric 11 are formed of the same material.

However, Harshfield (Fig. 24) further teaches that the first dielectric 110 and the second dielectric layer 122 formed within the opening are formed of the same material (column 13, lines 45-47). Accordingly, it would have been obvious to form the first dielectric layer and the second dielectric layer with either the different material or the same material because the changing the materials of the first and second dielectric layers would not change the functions of the device.

Regarding claims 16, 21, 31, 42 and 48, Morishita further discloses that the forming conductive layer step comprises substantially conformally depositing the conductive layer 10 on the sidewall surface and the bottom surface (see Fig. 1B).

Regarding claims 17, 19, 22, 32, 40, 43, 45, 49 and 51, Morishita further discloses that the removing step comprises substantially anisotropically etching such as reactive ion etching (column 4, lines 19-23) to form a conductive sidewall spacer 10 (see Fig. 1D).

Regarding claims 25-26, 35-36, 44, 46, 50 and 52, Morishita (Fig. 2) also discloses that the sidewall surface is the sidewall surface of the first dielectric layer 4, the second dielectric layer 12 is formed on the conductive layer 10 after the removing step (column 5, lines 10-15), and the second dielectric layer 12 is formed before the forming the upper level wiring conductor 7.

Regarding claims 58, 60, 63, 64, 69, 72, Morishita (Fig. 1D) further discloses that the conductive layer 10 has an area of contact with the upper level-wiring conductor, the area of contact having a dimension of about 1000 Angstroms (column 3, lines 54-60). Harshfield (Fig. 24) also teaches the conductive layer 124 has an area contact with the programmable resistance material 130, the conductive layer has a lateral dimension is small compared to the radius of the window 118 or 48 (column 13, lines 17-24), and the window 118 or 48 has a thickness of about 600 Angstroms (column 9, lines 30-33).

Regarding claims 59, 65, 68, and 73, Morishita (Fig. 1D) further discloses the portion of the bottom surface is a surface of a metal substrate 3.

5. Claims 61-62, 66-67, 70-71, and 74-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita and Harshfield as applied to claims (20, 40, 41, 47) above and further in view of Nagashima (US. 5,312,773).

Regarding claims 61, 66, 70, and 74, neither Morishita nor Harshfield disclose that the conductive layer comprises a dual-layered sidewall spacer.

However, Nagashima (Fig. 7) teaches the forming of a conductive layer on the sidewall surface and on a portion of the bottom surface of the opening, the conductive layer comprises a dual-layered conductive sidewall spacer of 42b/44b (not labeled, see Fig. 4). Accordingly, it would have been obvious to modified the method of forming the conductive layer 10 of Morishita by forming the conductive layer with a dual-layered conductive sidewall spacer because such dual-layered conductive sidewall spacer would provide a low contact resistance, as taught by Nagashima (column 5, lines 55-64).

Regarding claims 62, 67, 71, and 75, Nagashima (Fig. 7) further discloses that the dual-layered conductive sidewall spacer comprises two layers 42/44 of Ti/TiON (column 5, lines 55-57), one layer having a resistivity being less than the resistivity of the other.

Response to Arguments

6. Applicant argues that the combination of Morishita nor Harshfield does not suggest the limitations: "forming a conductive layer on said sidewall surface and a portion of said bottom surface, said portion being less than the entire bottom surface ... forming a programmable resistance material in electrical communication with said conductive layer."

This argument is not persuasive because as stated in the ground of rejection, Morishita's Fig. 1D clearly teaches the forming of a conductive layer 10 on the sidewall surface and a portion of the bottom surface, the portion being less than the entire bottom surface. And Harshfield (Fig. 24) teaches the forming of a phase-change programmable resistance material 130 of chalcogenide (column 7, lines 5-12 and column 14, lines 1-5) as an upper level-wiring conductor in electrical communication with a lower level-wiring conductor 106 through a conductive layer 124 (column 13, lines 48-51 and lines 66-67). Therefore, the combination of Morishita and Harshfield does suggest the invention as claimed.

Conclusion

Art Unit: 2814

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
April 2, 2007



PHAT X. CAO
PRIMARY EXAMINER